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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/002,009 | 12/05/2001 | Masao Shinozaki | XA-9590 | 3040 |

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| EXAMINER | |
|---|---|
| RAO, SHRINIVAS H | |
| ART UNIT | PAPER NUMBER |
| 2814 | |

DATE MAILED: 09/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/002,009 | SHINOZAKI ET AL. | |
| | Examiner | Art Unit | |
| | Steven H. Rao | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 June 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-7 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Priority*

Receipt is acknowledged of paper submitted under 35 U.S.C. 119(a)-(d), Japanese Patent Application No. 2000- 386088 filed December 19, 2000 which papers have been placed of record in the file.

### *Election/Restrictions*

Applicant's election without traverse of claims 1-7 and 21-26 in Paper No. 6 is acknowledged.

### *Preliminary Amendment Status*

Acknowledgment is made of entry of preliminary amendment filed 12/06/01 on entered on May 02, 2002.

Therefore claims 1,2 as originally filed, claims 3,4 as amended by the preliminary amendment; claims 5-6 as originally filed; claim 7 as amended by the preliminary amendment and claims 21-26 as recited in the preliminary amendment are currently pending in the application.

### *Specification*

### *Drawings*

The drawings filed along with the application on December 06, 2001 have been accepted by the draftsperson.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 1,2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1 the phrase "minimum processing dimension " renders the claim indefinite because the term "minimum processing dimension" cannot be determined from the is characterized according to applicant's own definition recited device claims that are not restricted to any particular method of/process of making the device.

Further, the specification while generally discussing the minimum processing dimension (a) in specification page 19, does not provide a clear explanation so that one skilled in the art can determine what applicants' intend to include/exclude by the recitation, " minimum processing dimension" in the claims.

Claims 3, 5-7 and 23 depend upon claim1 and are rejected at least for depending upon rejected claim 1.

Claims 4 21-22 and 24-26 depend upon claim 2 and are rejected at least for depending upon rejected claim 2.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patent ability shall not be negatived by the manner in which the invention was made.

Claims 1-7 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fifield et al. (U.S. Patent no. 6,166,561, herein after Fifield).

With respect to calim1, to the extent understood, Fifield describes a semiconductor device including an input circuit or an output circuit configured with a plurality of first MOS transistors (fig. 2 # VDD, col. 3 lines 30-32, col. 1 line 39); in a first area of a principal plane on a semiconductor substrate (fig. 2) and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on the semiconductor substrate (fig.2, area # 207 having transistors 219), wherein a spacing between a first gate electrode of the first MOS transistors constituting the input circuit or the output circuit and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a minimum processing dimension of the spacing between the first gate electrode and the first contact hole, for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a minimum processing dimension of the spacing between the first gate electrode and the first contact hole (fig. 3b the distance between VDDQ and the gate is larger than the distance between 311 and 303 b, col. 4 lines 63 to 67), and wherein spacing between a second gate electrode of

the second MOS transistors constituting the internal circuit and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors is equal to a minimum processing dimension of the spacing between the second gate electrode and the second contact hole.

Fifield does not specifically describe a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistor.

However, Fang, a patent from the same filed of endeavor, describes in fig. 6 and col. 3 lines 54-59 contact holes being formed in the insulating layer to connect the source /drain regions to an upper inter connect metal layer (wiring layer) and in figure 6 shows the spacing between spacing between a second gate electrode of the second MOS transistors constituting the internal circuit and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors is equal to a minimum processing dimension of the spacing between the second gate electrode and the second contact hole .

Therefore it would have been obvious to one of ordinary skill in the art the art at the time of the invention to include Fang's contact holes in Fairfield's device to form inter connects in multilevel moralization of devices.

With respect to claim 2, Fifiled describes a semiconductor device including an input circuit or an output circuit configured with a plurality of first MOS transistors in a first area of a principal plane on a semiconductor substrate, and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on the semiconductor substrate (fig.2, area # 207 having transistors 219), wherein a spacing between an edge of a first active

region in which the first MOS transistors constituting the input circuit or the output circuit are formed and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a minimum processing dimension of the spacing between the edge of the first active region and the first contact hole (fig. 3b the distance between VDDQ and the gate is larger than the distance between 311 and 303 b, col. 4 lines 63 to 67) and wherein a spacing between an edge of a second active region in which the second MOS transistors constituting the internal circuit are formed and a second contact hole for connecting a wiring to a source or a drain region of the second MOS transistors is equal to a minimum processing dimension of the spacing between the edge of the second active region and the second contact hole.

Fifield does not specifically describe a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistor.

However, Feng, a patent from the same filed of endeavor, describes in fig. 6 and col. 3 lines 54-59 contact holes being formed in the insulating layer to connect the source /drain regions to an upper inter connect metal layer (wiring layer) and in figure 6 shows the spacing between spacing between a second gate electrode of the second MOS transistors constituting the internal circuit and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors is equal to a minimum processing dimension of the spacing between the second gate electrode and the second contact hole .

Therefore it would have been obvious to one of ordinary skill in the art the art at the time of the invention to include Feng's contact holes in Fifield's device to form inter connects in multilevel metallization of devices.

With respect to claims 3 and 26, Fifiled describes a semiconductor device including a power supply voltage is applied to the first MOS transistors constituting the input circuit or the output circuit is equal (claim 3 , Fifield figs. 4A and B, col. 8 lines 17-48 ), higher (claim 26, Fifield figs. 4A-B, col. 8 line 49-65 ) to a power supply voltage applied to the second MOS transistors constituting the internal circuit.

With respect to claims 4, 22 and 23 Fifiled, describes a semiconductor device wherein a gate length of the first MOS transistors is equal to a gate length of the second MOS transistors.( Fifield fig. 3A distance between 307 and 317 is equal to the distance between gate in region215 and gate 351)

With respect to claims 5 and 24, a semiconductor device wherein a gate insulating film thickness of the first MOS transistors is equal to a gate insulating film thickness of the second MOS transistors. ( Feng col. 2 lines 41-42 and col . 3 lines 17-20).

With respect to claims 6 and 25, wherein Fifiled describes a semiconductor device wherein an area of the active region in which the first MOS transistors are formed is larger than an area of the active region in which the second MOS transistors are formed. ( Fifield fig. 3A)

With respect to claims 7 and 21, wherein a power supply voltage applied to the first MOS transistors constituting the input circuit or the output circuit is

higher (claim 7 Fifield figs. 4A-B, col. 8 line 49-65 ), equal (claim 21 Fifield figs. 4A and B, col. 8 lines 17-48) than a power supply voltage applied to the second MOS transistors constituting the internal circuit.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

August 17, 2002.

PHAT X. CAO
PRIMARY EXAMINER